PRELIMINARY

82730
TEXT COPROCESSOR

- **High Quality Display for Text Applications**
- **Provides Proportional Spacing, Alphamosaic Graphics, Simultaneous Superscript/Subscript and Soft Font Support**
- **High Performance Text Manipulation Through 4 Mbytes/sec DMA, Bus Interface, Processing Unit and Dual Row Buffers (Up to 200 Characters Each)**
- **Programmable Bus Interface Handles 8 or 16 Bit Data and 16 or 32 Bit Addressing; iAPX 86/88/186/188 Compatible**
- **On-Chip Processing Unit Simplifies Software Design by Executing High Level Commands and Supporting Linked List Data Structures**
- **Extremely Flexible; Programmable Features Include Screen and Row Formats, Two Cursors, Character and Field Attributes and Smooth Scrolling**
- **Simultaneous Display of Independent Data Bases Through Programmable Virtual Screen Mode**
- **High Resolution Display; Up to 200 Characters per Row and 2048 Scan Lines per Frame**
- **Separate Bus and Video Clocks Allow Optimization of Overall System Performance**
- **Provides a Complete LSI Solution for Display Control when Used in Conjunction with the 82731 Video Interface Controller**

The 82730 Text Coprocessor is a high performance VLSI solution for raster scan text oriented displays. The 82730 works as a coprocessor and has processing capabilities specifically tailored to execute data manipulation and display tasks. It provides the designer the ability to functionally partition his system thereby offloading the system CPU and achieving maximum performance through concurrent processing. The 82730 supports the generation of high quality text displays through features like proportional spacing, simultaneous superscript/subscript, dynamically reloadable fonts and user programmable field and character attributes. An intelligent system interface and efficient software capabilities makes 82730 based systems easy to design. In addition, when coupled with the 82720 Graphics Display Controller, the 82730 provides flexible mixing of high quality text and graphics simultaneously on the same display.

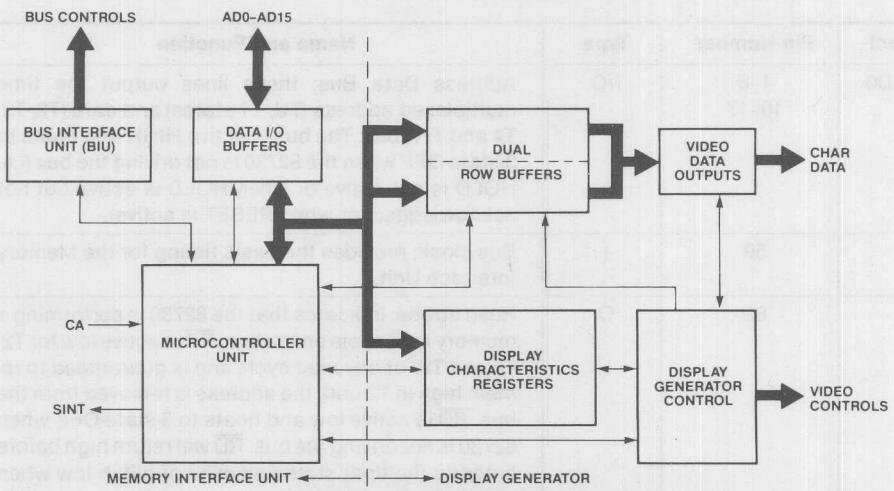

Figure 1. 82730 Block Diagram

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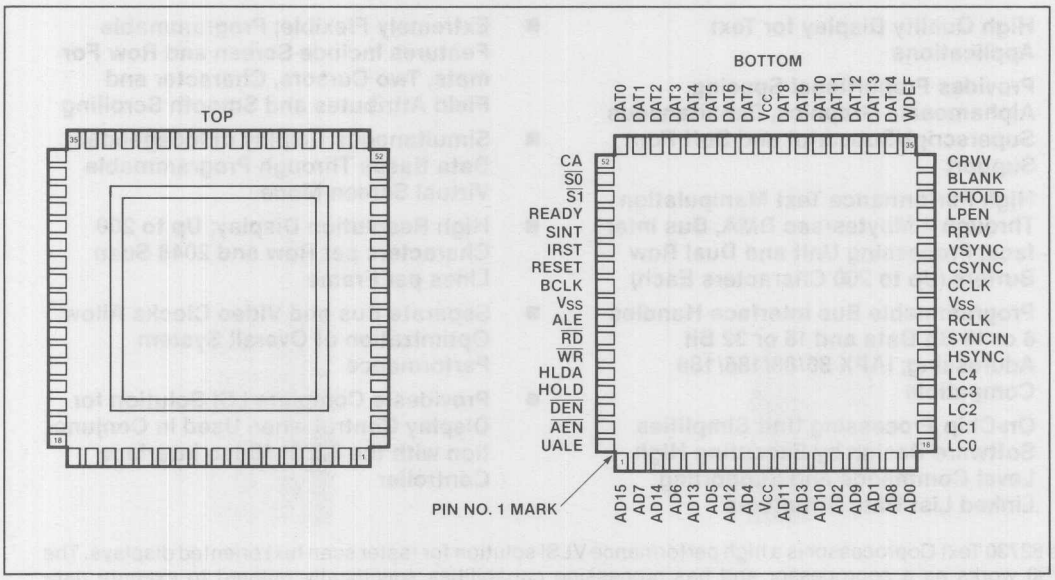


Figure 2. 82730 Pinout Diagram

Table 1. 82730 Pin Description

The 82730 is packaged in a 68 pin JEDEC Type A ceramic package.

Symbol	Pin Number	Type	Name and Function
AD15–AD0	1–8 10–17	I/O	Address Data Bus; these lines output the time multiplexed address (TU, T1 states) and data (T2, T3, T4 and TW) bus. The bus is active HIGH and floats to 3-state OFF when the 82730 is not driving the bus (i.e. HOLD is not active or when HOLD is active but not acknowledged, or when RESET is active).
BCLK	59	I	Bus clock; provides the basic timing for the Memory Interface Unit.
$\overline{RD}$	62	O	Read strobe; indicates that the 82730 is performing a memory read cycle on the bus. $\overline{RD}$ is active low for T2, T3 and TW of any read cycle and is guaranteed to remain high in T2 until the address is removed from the bus. $\overline{RD}$ is active low and floats to 3-state OFF when 82730 is not driving the bus. $\overline{RD}$ will return high before entering the float state and will not glitch low when entering or leaving float.

Table 1. 82730 Pin Description (Continued)

Symbol	Pin Number	Type	Name and Function
$\overline{WR}$	63	O	Write strobe; indicates that the data on the bus is to be written in a memory device. $\overline{WR}$ is active for T2, T3 and TW of any write cycle. It is active LOW and floats when 82730 is not driving the bus. $\overline{WR}$ will return high before entering the float state and will not glitch low when entering or leaving float.
ALE	61	O	Lower Address Latch Enable; provided by the 82730 to latch the address into an external address latch such as 8282/8283 (active HIGH). Addresses are guaranteed to be valid on the trailing edge of ALE.
UALE	68	O	Upper Address Latch Enable; it is similar to ALE except that it occurs in upper address output cycle (TU).
$\overline{AEN}$	67	O	Address Enable; $\overline{AEN}$ is active LOW during the entire period when 82730 is driving the bus. It can be used to unfloat the outputs of the Upper and Lower Address latches.
$\overline{DEN}$	66	O	Data enable; provided as a data bus transceiver output enable for transceivers like the 8286/8287. $\overline{DEN}$ is active LOW during each bus cycle and floats when 82730 is not driving the bus. $\overline{DEN}$ will not glitch when entering or leaving the float state.
$\overline{S0}$, $\overline{S1}$	53, 54	O	Status pins; encoded to provide bus-transaction information: $\overline{S1}$ $\overline{S0}$ Bus Cycle Initiated 0 0 - - - (Reserved) 0 1 Memory Read 1 0 Memory Write 1 1 Passive (No bus cycle) These pins are directly compatible with iAPX 86, 186 status outputs $\overline{S1}$ and $\overline{S0}$. The status pins are floated when 82730 is not driving the bus. They will not glitch when entering or leaving the 3-state condition.
READY	55	I	READY; signal to inform the 82730 that the data transfer can be completed. Immediately after RESET, READY is asynchronous (internally synchronized) but can be programmed during initialization to bus synchronous.

Table 1. 82730 Pin Description (Continued)

Symbol	Pin Number	Type	Name and Function
HOLD	65	O	HOLD; indicates that the 82730 wants bus access. HOLD stays active HIGH during the entire period when 82730 is driving the bus.
HLDA	64	I	Hold Acknowledge; indicates to 82730 that it is granted the bus access as requested. HLDA may be asynchronous to 82730 clock. If HLDA goes inactive (LOW) in the middle of an 82730 bus cycle, the 82730 will complete the current bus cycle first, then it will drop HOLD and float address and bus control outputs.
CA	52	I	Channel Attention; used to notify 82730 that a command in the command block is waiting to be processed. CA is latched on its falling edge.
SINT	56	O	Status Interrupt; used to inform the processor that an unmasked interrupt has been generated in the 82730 status register.
IRST	57	I	Interrupt Reset; SINT is cleared by activating the IRST pin.
RESET	58	I	Reset; causes 82730 to immediately terminate its present activity and enter a dormant state. The signal must be active HIGH for at least 4 BCLK cycles and is internally synchronized to the bus clock.
CCLK	27	I	Character clock; input used to clock row buffer data, attribute, cursor and line count out of 82730. When more than one 82730 is connected in cluster mode, CCLK is used to synchronize output from both master and slave chips. A character data word will be output at every rising edge of CCLK.
RCLK	25	I	Reference clock; input used to generate timings for the screen layout and to define screen columns for data formatting. All raster output signals are specified relative to the rising edge of RCLK.
DAT0-DAT14	36-42 44-51	O	Video data bus output; the least significant 15 bits of the character data words are passed through the 82730 row buffer and made available on the pins DAT0-DAT14. The user has the flexibility to partition the data word into character and attribute bits per his requirements. The bits that are assigned for internally generated attributes may also be available at pin DAT0-DAT14. New character data will be shifted to these output pins at every rising edge of the CCLK. Together with LC0-LC4, they may be used to address the character generator or as attribute controls.

Table 1. 82730 Pin Description (Continued)

Symbol	Pin Number	Type	Name and Function
WDEF	35	O	Width Defeat; is used to indicate when the character is allowed to be a variable width or must be of fixed width. WDEF is LOW if the character being output is normal, but is HIGH if it is a superscript/subscript character or visible attribute (TAB or GPA). Optionally, WDEF can be held high by user command.
LC0-LC4	18-22	O	Line count outputs; used to address the character generator for the line positions in a row. The line number output is a function of the display mode and character attributes programmed by the user.
CSYNC	28	O	CCLK synchronization output; used to synchronize external character clock generator to reference clock timing. This output is active (high) outside the display field.
$\overline{\text{CHOLD}}$	32	O	CCLK Inhibit output; used by external logic to inhibit CCLK generation. This output is active (low) during the tab function.
SYNCIN	24	I	Synchronization input; used to synchronize the vertical timing counters to an externally generated VSYNC signal. Used by slave mode 82730 to synchronize to a master mode 82730 and by the master 82730 to lock the frame to an external source such as the power line frequency.
HSYNC	23	O (MASTER) I (SLAVE)	Horizontal Sync; in master mode, it is used to generate the CRT monitor's horizontal sync signal. It is active HIGH during the programmed horizontal sync interval. In interlace slave mode it is used in conjunction with SYNCIN to indicate the start of the even field for timing counter reset. At RESET, pin is set as an output in the LOW state.
VSYNC	29	O	Vertical Sync; active HIGH during the programmed vertical sync interval and used to generate the CRT monitor's vertical sync signal.
BLANK	33	O	Blanking output; used to suppress the video signal to the CRT. BLANK is clocked by CCLK.
CRVV	34	O	Character Reverse Video (CCLK output); used to externally invert video data output. CRVV is clocked by CCLK.
RRVV	30	O	Reference Reverse Video (RCLK output); to externally invert video in the field and border area if so programmed by user. It is LOW outside the border area, RRVV is clocked by RCLK.

Table 1. 82730 Pin Description (Continued)

Symbol	Pin Number	Type	Name and Function
LPEN	31	I	Light Pen Input; used to latch the position of a light pen. At the rising edge of this input, the column position and the row position of the 82730 will be loaded into the LPENROW and LPENCOL locations in the Command block.
V_{CC}	9, 43		Power; +5 volts nominal potential.
V_{SS}	26, 60		Power; ground potential.

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the 82730. The chip is divided into two main sections—The Memory Interface Unit (MIU) and the Display Generator (DG). The MIU provides the communication between the 82730 and system processor and memory, while the DG acts on the display data and carries out the display operation.

Communication between the 82730 and the CPU takes place through messages placed in communication blocks in shared memory. The processor issues channel commands by preparing these message blocks and directing the 82730's attention to them by activating a hardware channel attention signal (CA). The MIU fetches and executes these commands. When the display process is activated, the 82730 repeatedly fetches display data and embedded datastream commands from memory utilizing its built-in DMA capability, executes any datastream commands as encountered on the fly, and loads the row buffers with the display data. After executing these commands, the 82730 clears a busy flag in memory, to inform the host CPU that it is ready for the next command.

The MIU is divided into two sections—The Bus Interface Unit (BIU) and the Micro Controller Unit (MCU). The BIU provides the electrical interface to the system bus, and the timing signals required for the MCU operations, making these operations transparent to the MCU. The 82730 can be programmed during initialization to provide 8 or 16 bit data, and 16 or 32 bit addressing.

The MCU contains the microinstruction store and the associated circuitry required for the execution of all channel and datastream commands. It uses the BIU in carrying out its memory access tasks such as loading the row buffers with display data.

The interaction between the MCU and the DG takes place through shared internal storage. The MCU fetches data from memory and writes it in the internal storage, while the DG reads from the internal storage and carries out the display operation. The MCU and DG operate asynchronously with respect to each other. Synchronization is accomplished through communication via internal flags and display timing signals generated by the DG. The internal shared storage consists of Row Buffers which store the display data and internal registers which store display parameters. There are two row buffers each capable of storing up to 200 characters. The data in one row buffer is used by the DG to display one complete character row on the screen, while the MCU is loading the second row buffer with display data fetched from memory. At the end of the row being displayed, the buffers are swapped and the MCU and DG resume their respective tasks.

The Display Characteristics Registers contain all the information used to control every aspect of display characteristics from screen size to blink rates. A major portion of this register set is the three Content Addressable Memory (CAM) arrays that allow very flexible timing control for row and screen characteristics. The user has the power to set the parameters for the entire screen by invoking a single high level command.

By separating the Video Interface clocks from the Bus Interface clock, the 82730 provides the designer the ability to independently maximize the performance of the CPU and Video sections of the system.

The Video interface consists of two independent clocks: the Reference Clock (RCLK) and the Character Clock (CCLK). While the RCLK controls the raster timing and defines the screen layout, the

CCLK independently shifts character and attribute information out of the 82730, which allows proportional spacing to be achieved.

It is this combination of hardware features and high level command interface that makes the 82730 the first VLSI Text Coprocessor which simplifies hardware design and software development.

Table 2. 82730 Command Summary

DATA STREAM COMMANDS	
Name	**Function**
EOR	End DMA for this (virtual) row. Resume DMA on the next row with the same data string
EOF	End DMA for this frame (virtual window)
EOL	End DMA for this (virtual) row. Resume DMA with the next data string
FULROWDESCRPT	Redefine row heights, character position, etc. for the row being affected by DMA*
SL SCROLL STRT	Define the beginning of a scrolled window and the amount of scrolling of the top row*
SL SCROLL END	Define the end of a scrolled window* and the amount of scrolling of the bottom row
TAB TO N	Set a tab location at reference clock position N*
LD MAX DMA COUNT	Set a limit on the maximum characters to be fetched for this and subsequent (virtual) rows*
EOS	Direct DMA to the next string and continue DMA (No EOR)
SKIP N	Do not fetch next N characters. Commands are executed (except set general-purpose attribute and tab)
REPEAT N	Repeat the next character N times
SUB SUP N	The next N pairs of characters are displayed as superscripts and subscripts
RPT SUB SUP	The next N pairs of characters are repeated N times as superscripts and subscripts
SET GPA	Redefine 4 character code output pins as normal or general-purpose attribute pins
SET FIELD ATTRIBUTE	Set the field attribute mask to cause setting of character data on a field basis
INIT NEXT PROCESS	Initialize virtual display window (virtual display only)*
NOP	No operation (user-available command codes)

*In virtual display mode these instructions are interpreted as NOPs.

Table 2. 82730 Command Summary (Continued)

CHANNEL COMMANDS	
Name	**Function**
NOP	No operation
START DISPLAY	Start DMA of data and display functions
START VIRTUAL DISPLAY	Start virtual display DMA and display
STOP DISPLAY	Stop DMA and display
MODESET	Load display parameters from mode block
LOAD CBP	Direct 82730 to a new command block
LOAD INTMASK	Load new value to interrupt mask register from command block
LPEN ENABLE	Enable light pen input
READ STATUS	Direct 82730 to write its status register to command block
LD CUR POS	Load new cursor positions from command block
SELF TEST	Direct 82730 to run internal self-test diagnostics
TEST ROW BUFFER	Direct 82730 to test row buffer memory using data in system memory

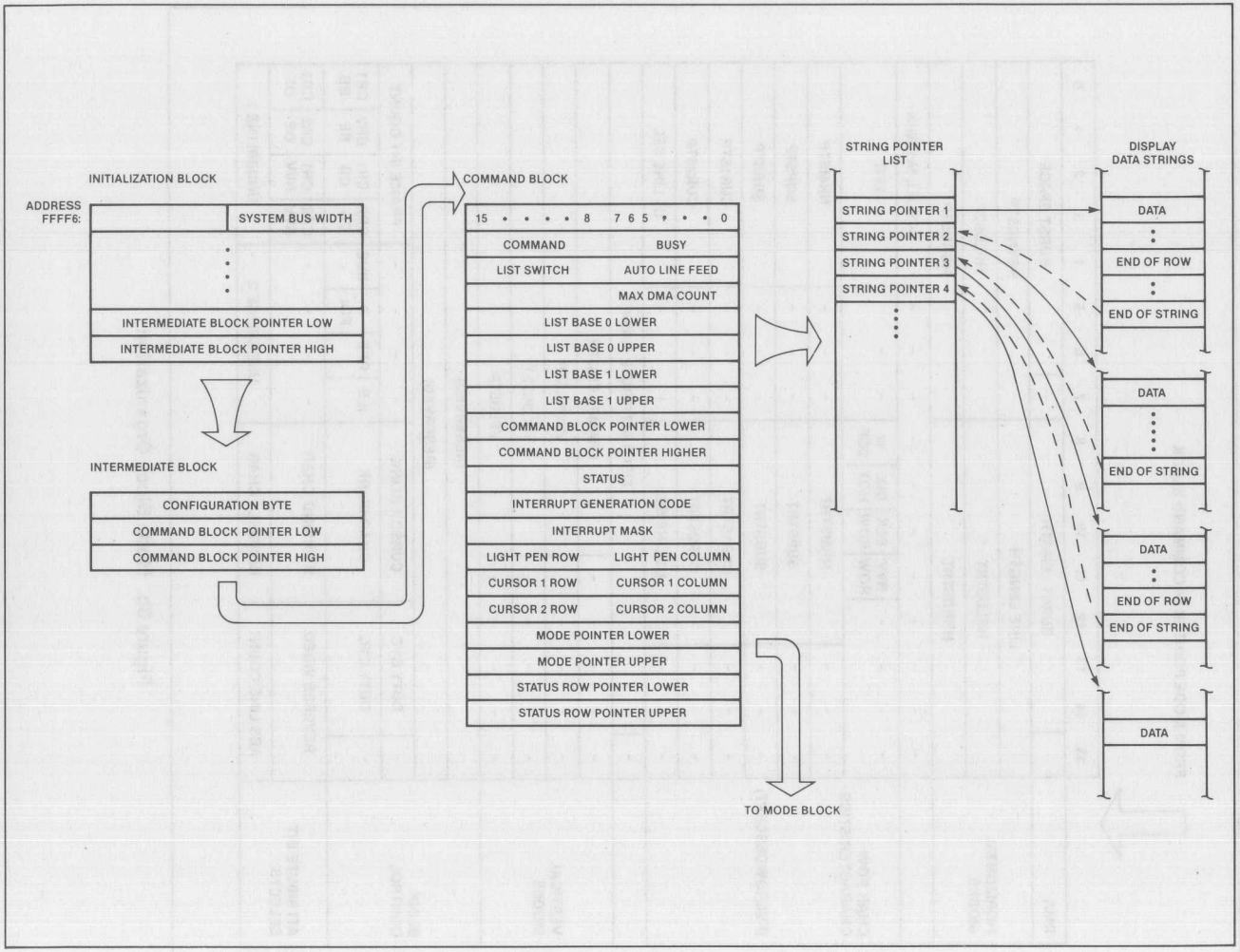
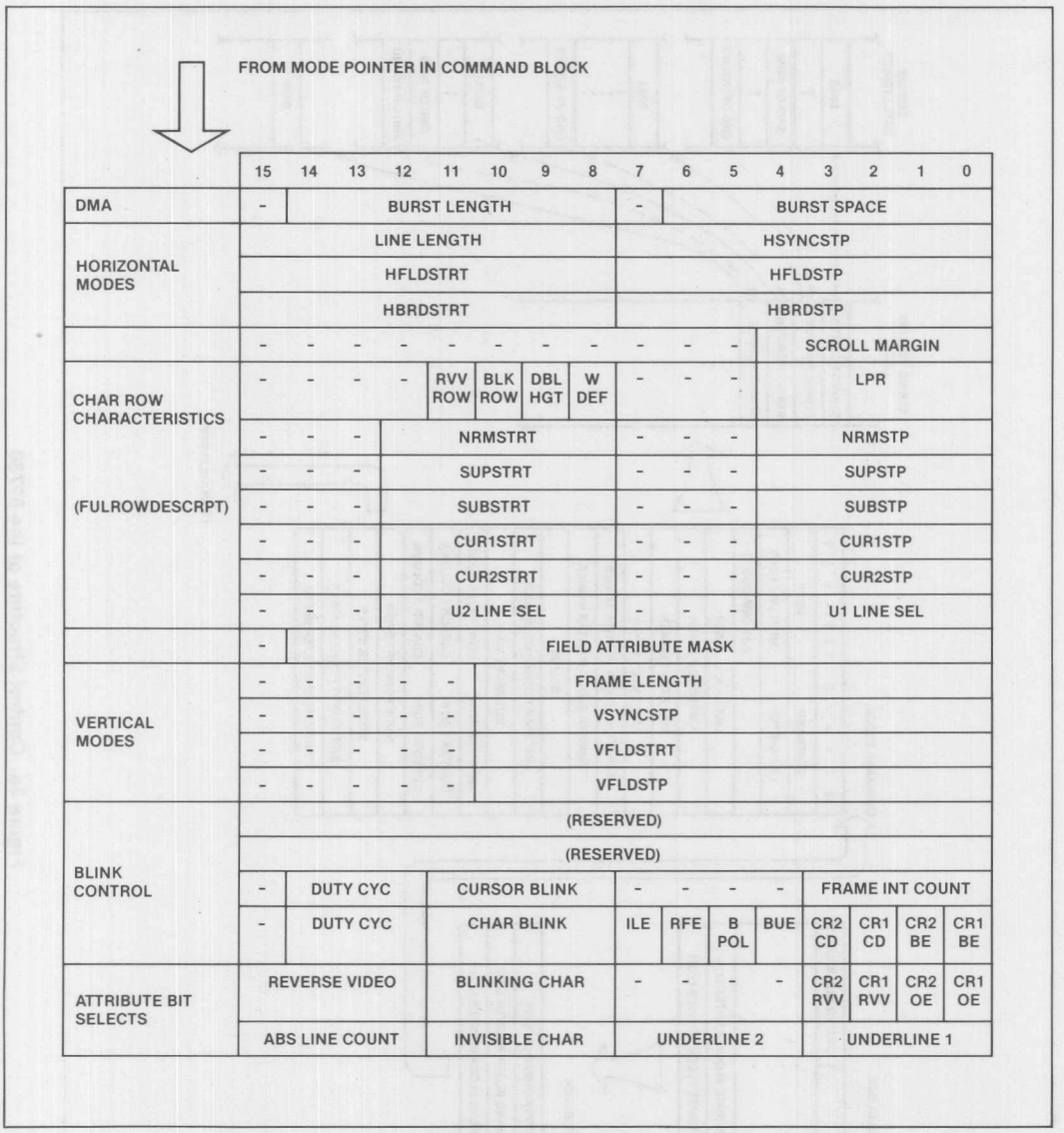


Figure 3a. Control Structure of the 82730



	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA	-	BURST LENGTH							-	BURST SPACE						
HORIZONTAL MODES	LINE LENGTH								HSYNCSTP							
	HFLDSTRT								HFLDSTP							
	HBRDSTRT								HBRDSTP							
	-	-	-	-	-	-	-	-	-	-	-	SCROLL MARGIN				
CHAR ROW CHARACTERISTICS	-	-	-	-	RVV ROW	BLK ROW	DBL HGT	W DEF	-	-	-	LPR				
	-	-	-	NRMSTRT					-	-	-	NRMSTP				
	-	-	-	SUPSTRT					-	-	-	SUPSTP				
(FULROWDESCRPT)	-	-	-	SUBSTRT					-	-	-	SUBSTP				
	-	-	-	CUR1STRT					-	-	-	CUR1STP				
	-	-	-	CUR2STRT					-	-	-	CUR2STP				
	-	-	-	U2 LINE SEL					-	-	-	U1 LINE SEL				
	-	FIELD ATTRIBUTE MASK														
VERTICAL MODES	-	-	-	-	-	FRAME LENGTH										
	-	-	-	-	-	VSYNCSTP										
	-	-	-	-	-	VFLDSTRT										
	-	-	-	-	-	VFLDSTP										
BLINK CONTROL	(RESERVED)															
	(RESERVED)															
	-	DUTY CYC		CURSOR BLINK					-	-	-	-	FRAME INT COUNT			
	-	DUTY CYC		CHAR BLINK					ILE	RFE	B POL	BUE	CR2 CD	CR1 CD	CR2 BE	CR1 BE
ATTRIBUTE BIT SELECTS	REVERSE VIDEO			BLINKING CHAR					-	-	-	-	CR2 RVV	CR1 RVV	CR2 OE	CR1 OE
	ABS LINE COUNT			INVISIBLE CHAR					UNDERLINE 2				UNDERLINE 1			

Figure 3b. Mode Block Organization

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias .... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0V to +7V
Power Dissipation ..... 3 Watts

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	Volts	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	$I_{OL} = 2$ mA [1]
V_{OH}	Output High Voltage	2.4		Volts	$I_{OH} = -400\ \mu A$
I_{CC}	Power Supply Current		400	mA	$@T_A = 0°C$
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = 0 - V_{CC}$
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = 0.45 - V_{CC}$
V_{BLI}	Bus Clock Input Low Voltage	−0.5	0.8	Volts	
V_{BHI}	Bus Clock Input High Voltage	2.0	$V_{CC}+1.0$	Volts	
V_{CLI}	Character Clock Input Low Voltage	−0.5	0.8	Volts	
V_{CHI}	Character Clock Input High Voltage	2.0	$V_{CC}+0.5$	Volts	
V_{RLI}	Reference Clock Input Low Voltage	−0.5	0.8	Volts	
V_{RHI}	Reference Clock Input High Voltage	2.0	$V_{CC}+0.5$	Volts	

NOTE:
1. $I_{OL} = 2.6$ mA on the $\overline{S1}$ and $\overline{S0}$ pins.

A.C. CHARACTERISTICS

82730 Bus Interface Input Timing Requirements
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$. All timings in nanoseconds.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLCL	BCLK Cycle Period	125	2000	ns	
TCLCH	BCLK Low Time	52		ns	
TCHCL	BCLK High Time	52		ns	
TCH1CH2	BCLK Rise Time		30	ns	0.45V→2.4V
TCL1CL2	BCLK Fall Time		30	ns	2.4V→0.45V
TDVCL	Data in Set-Up Time	20		ns	

A.C. CHARACTERISTICS (Continued)

82730 Bus Interface Input Timing Requirements (Continued)
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$. All timings in nanoseconds.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLDX	Data on Hold Time	10		ns	
TARYHCH	Async. READY Active Set-Up Time	35		ns	
TSRYHCL	Sync. READY Active Set-Up Time	– 10		ns	
TRYLCL	READY Inactive Set-Up Time	0		ns	
TCLRYX	READY Hold Time	20		ns	
TCTVCL	HLDA, RESET Set-Up Time	35		ns	
TCLCTX	HLDA, RESET Hold Time	10		ns	
TCAVCAX	CA Pulse Width	TCLCL		ns	

82730 Bus Interface Output Timing Response
$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$. All timings in nanoseconds. $C_L = 200$ pF except on ALE where $C_L = 100$ pF

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLAV	Address Valid Delay	0	60	ns	
TCLAX	Address Hold Time	0		ns	
TAVAL	Address Valid to ALE/UALE Inactive	TCLCH – 30		ns	
TLLAX	Address Hold to ALE Inactive	TCHCL – 10		ns	
TCLAZ	Address Float Delay	TCLAX	45	ns	
TAZRL	Address Float to $\overline{RD}$ Active	0		ns	
TLHLL	ALE/UALE Width	TCLCH – 10		ns	
TCLLH	ALE/UALE Active Delay	0	45	ns	
TCHLL	ALE/UALE Inactive Delay	0	45	ns	
TCVCTV	Control Active Delay ($\overline{DEN}$,$\overline{WR}$,$\overline{AEN}$)	0	70	ns	
TCVCTX	Control Inactive Delay ($\overline{DEN}$,$\overline{WR}$,$\overline{AEN}$)	0	65	ns	
TCLDOV	Data Out Valid Delay	0	55	ns	
TCLDOX	Data Out Hold Time	0		ns	
TDWHDOX	Data Out Hold Time After $\overline{WR}$	TCLCL – 60		ns	
TCLHV	Hold Output Delay	0	85	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL – 50		ns	
TCLRL	$\overline{RD}$ Active Delay	0	95	ns	
TCLRH	$\overline{RD}$ Inactive Delay	0	70	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL – 40		ns	

A.C. CHARACTERISTICS (Continued)

82730 Bus Interface Output Timing Response (Continued)

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$. All timings in nanoseconds. $C_L = 200$ pF except on ALE where $C_L = 100$ pF

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCLSIN	SINT Valid Delay	0	70	ns	
TRIHSIL	RINT Active to SINT Inactive		250	ns	
TCHSV	Status Active Delay	0	60	ns	
TCLSH	Status Inactive Delay	0	70	ns	
TWLWH	$\overline{WR}$ Width	2TCLCL – 40		ns	
TFLHL	Bus Float to HOLD Inactive	0		ns	

82730 Display Generator Input Timing Requirements

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$. All timings in nanoseconds. $C_L = 100$ pF except where noted.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TRCHRCH	RCLK Cycle Period	100	2500	ns	
TRCHRCL	RCLK High Time	40		ns	
TRCLRCH	RCLK Low Time	40		ns	
TRRCK	RCLK Rise Time		30	ns	0.45V→2.4V
TFRCK	RCLK Fall Time		30	ns	2.4V→0.45V
TCCHCCH	CCLK Cycle Period	100	None	ns	
TCCHCCL	CCLK High Time	30		ns	
TCCLCCH	CCLK Low Time	40		ns	
TRCCK	CCLK Rise Time		30	ns	0.45V→2.4V
TFCCK	CCLK Fall Time		30	ns	2.4V→0.45V
TSYVCR	SYNCIN Set-Up Time to RCLK in Slave Mode		30	ns	

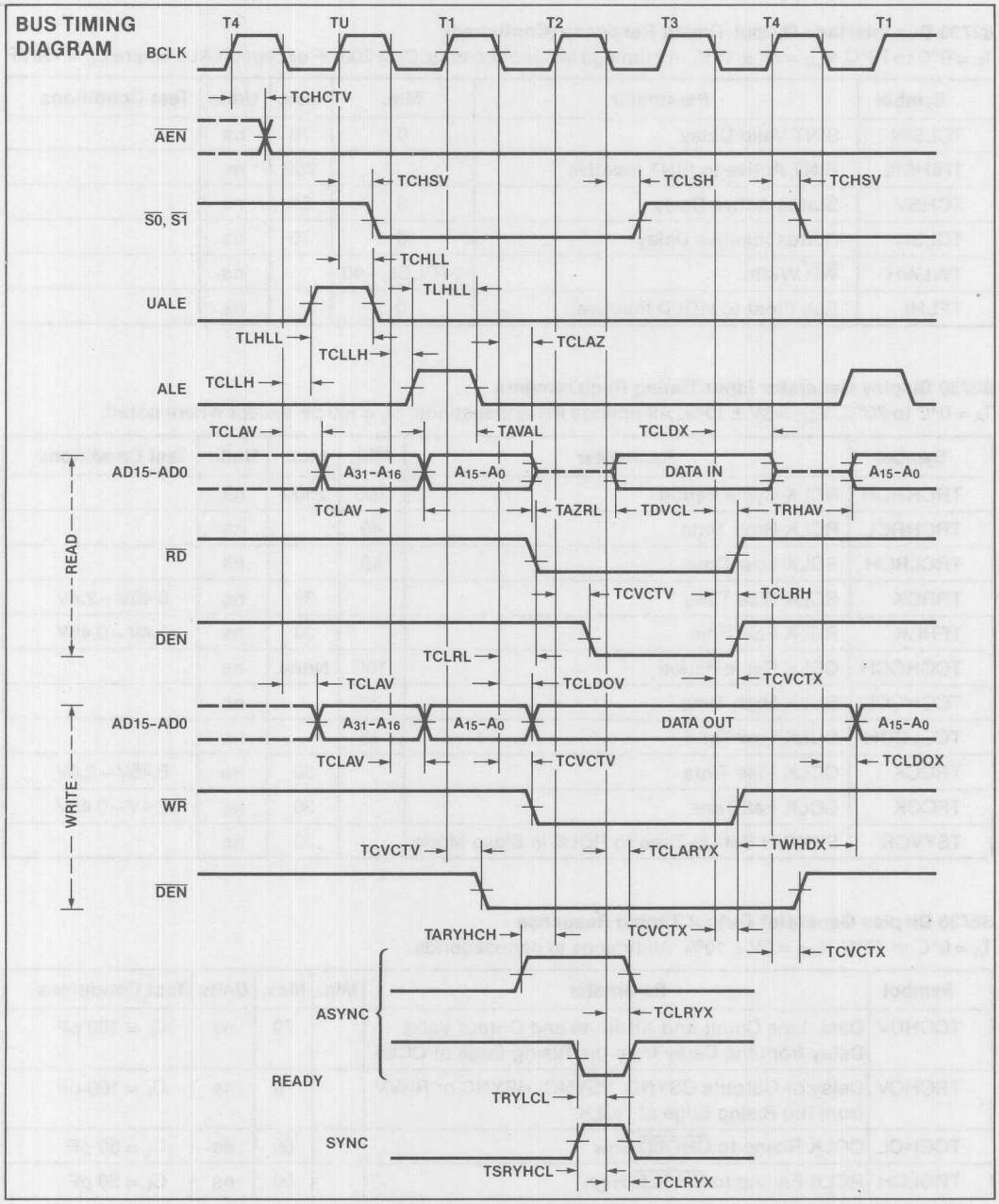
82730 Display Generator Output Timing Response

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$. All timings in nanoseconds.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TCCHDV	Data, Line Count and Attribute and Output Valid Delay from the Delay from the Rising Edge of CCLK		70	ns	$C_L = 100$ pF
TRCHCV	Delay of Outputs CSYNC, VSYNC, HSYNC or RRVV from the Rising Edge of RCLK		70	ns	$C_L = 100$ pF
TCCHCL	CCLK Rising to $\overline{CHOLD}$ Low		60	ns	$C_L = 50$ pF
TRCLCH	RCLK Falling to $\overline{CHOLD}$ High		60	ns	$C_L = 50$ pF

WAVEFORMS

BUS TIMING DIAGRAM



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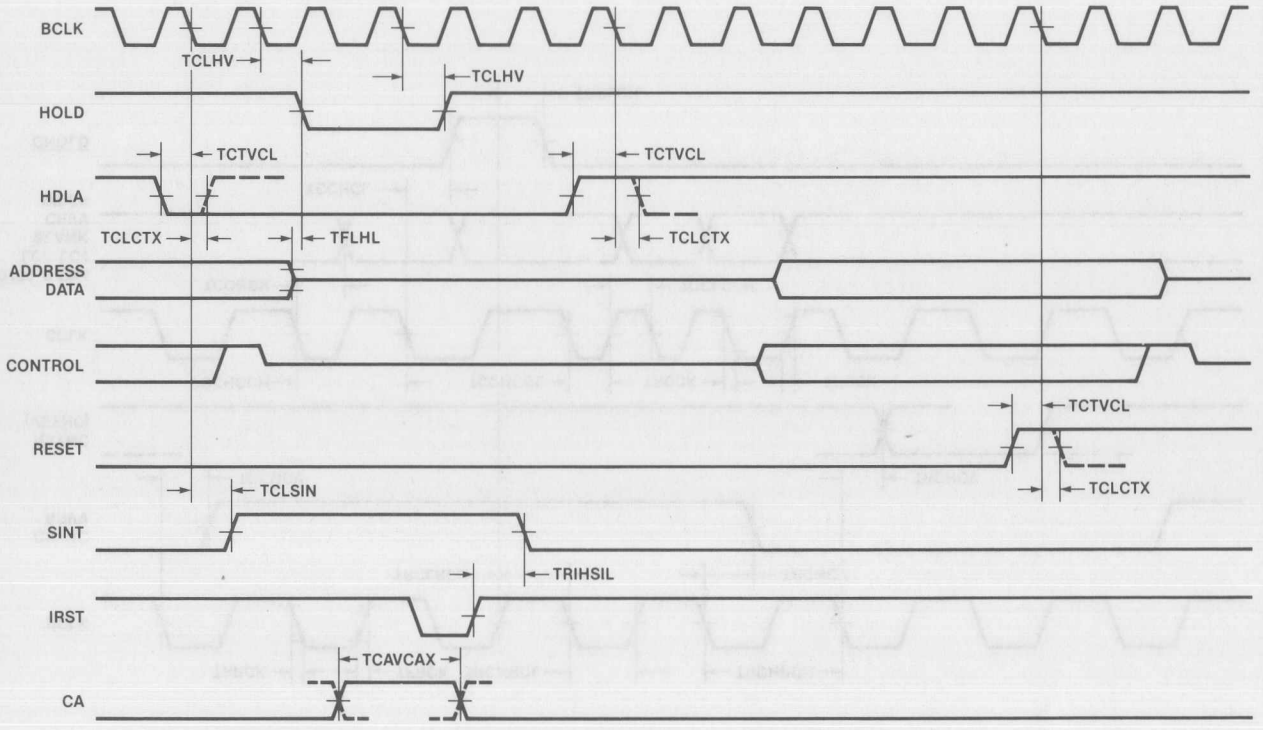
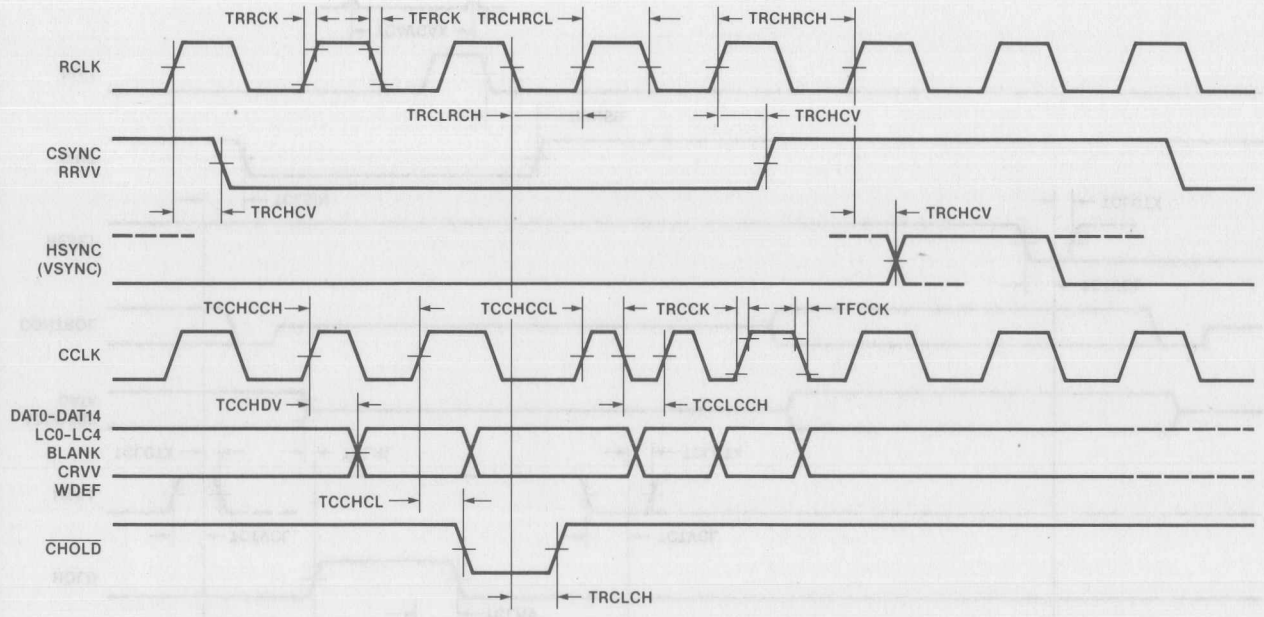
WAVEFORMS (Continued)

HOLD, RESET, SINT AND CA TIMING



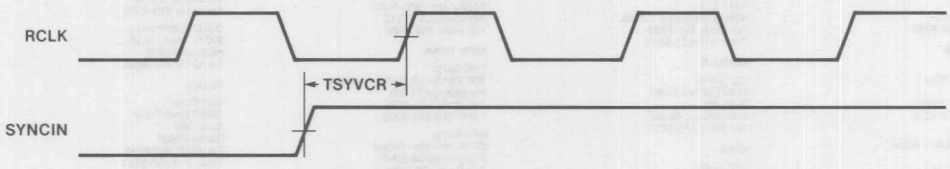
WAVEFORMS (Continued)

DISPLAY GENERATOR INTERFACE TIMING



WAVEFORMS (Continued)

SYNCIN TIMING



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*Field Application Location